

pplicant: Rammel Attorney Docket No. BING-1-1032

Serial No.: 10/720,614 Group Art Unit: Not yet assigned

Filing Date: November 24, 2003 Examiner: Not yet assigned

Title: METHODS AND APPARATUS FOR SIMULATION SPEEDUP

INFORMATION DISCLOSURE STATEMENT

Commissioner For Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

Pursuant to 37 C.F.R. § 1.56 and in accordance with 37 C.F.R. §§1.97-1.98, information related to the above-identified application is hereby disclosed. Inclusion of information in this statement is not to be construed as an admission that this information is material as that term is defined in 37 C.F.R. § 1.56(b).

In accordance with §1.97(b), since this Information Disclosure Statement is being filed either within three months of the filing date of the above-identified application, within three months of the date of entry into the national stage of the above identified application as set forth in §1.491, or before the mailing date of a first Office Action on the merits of the above-identified application, no additional fee is required.

Copies of references listed on the attached Form PTO-1449 are enclosed herewith, along with a return receipt postcard.

Respectfully submitted,

BLACK LOWE & GRAHAMPLLC

Dale C. Barr

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Direct Dial: 206.957.2463

BING-1-1032TL02



MAIL CERTIFICATE

I hereby certify that this communication is being deposited with the United States Postal Service via first class mail under 37 C.F.R. § 1.08 on the date indicated below addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

2/24/04

Date of Deposit

Jennifer J. Fortuny

25315 CUSTOMER NUMBER - 2 -

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BING-1-1032TL02

BANNIFORMATION DISCLOSURE STATEMENT BY APPLICANT					Complete if Known		
					Application Number	10/720,614	
					Filing Date	November 24, 2003	
STATEMENT BY AFFEIGANT				, A14 I	First Named Inventor	First Named Inventor Rammel	
					Group Art Unit	oup Art Unit Not yet assigned	
					Examiner Name	Not yet assigned	
Sheet	1		of	1	Attorney Docket Number	BING-1-1032	
NON PATE	NT LITE	RATU	IRE DOC	UMENTS			
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published					
	1.	CANTLE A. J., and DEVLIN M., "A Foundation Architecture For Elevating DSP in FPGAs," Nallatech Ltd, Glasgow, Scotland, MAPLD Technical Program 1999, Paper B4, pp. 1-9, www.nallatech.com. http://www.mathworks.com/products/simulink/, "Xilinx System Generator for DSP, version 3.1," The MathWorks, Inc., 1994-2003, Web link 1 page, User Guide pp. 1-236.					
	2.						
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Date

Considered

Examiner

Signature

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

^{1.} Applicant's unique citation designation number (optional). 2. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22315-1450. DO NOT SEND FEES OR COMPLETED FORMSTO THIS ADDRESS. SEND TO: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22315-1450.